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Characterization of 6T SRAM Cell ACROSS Process, Voltage and Temperature Corners

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Abstract—*With the shift of the center of mass of the semiconductor industry towards consumer, multimedia and communications applications, different needs in terms of memory have risen. The unprecedented hunger for more memory is the mostly driven by the computer industry. Power consumption is becoming a limiting factor on the how much memory can be integrated on a single die.*
In this paper we have analyzed and charaterised the 6 transistor SRAM cell across process, voltage and temperature variations. The SRAM parameters considered are Read Delay, Write Delay, SNM Read , SNM write and leakage power dissipation.

1. INTRODUCTION

Static Random Access Memories (SRAM) are a vital component of many VLSI chips. Memories are widely used in all electrical and electronics systems viz : mainframes, microcomputers and cellular phones etc. with technology process maturing in submicron region to support Moore's Law, memory capacity on a chip is increasing day by day. This is true for microprocessors and microcontrollers, where the memory sizes are increasing with each generation to bridge the growing gap in the speeds of the processor and the main memory. [4]

Moreover, power consumption has become an important consideration both due to the increased level of integration and operating speeds as well as due the tremendous growth of battery operated devices. This paper focuses on characterization of 6T SRAM cell in 0.18µm in CMOS technology.

Where process and supply scaling remain the biggest drivers of low power designs, this work investigates some techniques which can be used in conjunction to scaling to achieve low power operation.

The main objective of this paper is to design 6T SRAM cell and optimize for read and write performance. The second objective is to characterize this SRAM cell across process, voltage and temperature corners.

2. LITERATURE REVIEW

2.1 6T SRAM Cell

HIGH-PERFORMANCE SRAM's are a crucial component in the memory hierarchy of current computing systems. This design focuses on three parameters process voltage and temperature variations in 0.18µm CMOS technology.

For process variations TSMC 180nm CMOS process has been taken into consideration. Process variations can result in the following combinations viz : typical nmos - typical pmos , slow nmos – slow pmos, fast nmos – fast pmos , slow nmos – fast pmos and fast nmos – slow pmos.

Another issue is temperature, i.e., normally devices are perform their best at -4°C to 60°C. So normally face problem in cold place there temperature is less then -4°C. The proposed project will operate at -20°C to 80°C temperature.

Another parameter is voltage. The designed SRAM cell works with supply voltage of 1.8V ±10%.

The proposed work develops simple mathematical models for process, voltage and temperature for the 6T SRAM cell and the verify these against SPICE circuit simulations. The technology under consideration for this analysis is a 0.18 µm CMOS TSMC process.

2.2 6T SRAM Cell Working

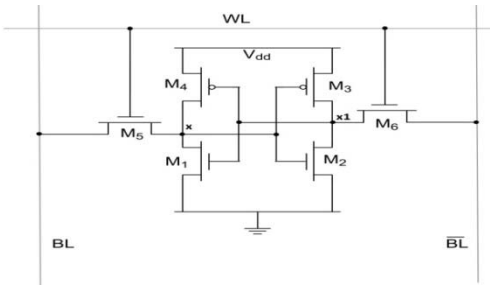

Fig. 1: 6T SRAM Cell

A switch-level circuit of the conventional 6T SRAM storage cell is shown here. The above memory cell forms the basis for most static random-access memories . Six transistors are utilized to store and access one bit of data. The four transistors in the center form two cross-coupled inverters. In real devices, these transistors are made in minimum feature sizes to reduce circuit area. Due to the cross coupled structure, a low input voltage value on the first inverter will generate a high voltage value on the second inverter, which increases and saves the low voltage value on the second inverter. Likewise, a high input voltage value on the first inverter will generate a low input voltage value on the second inverter, which is feedback as the low input value onto the first inverter. Therefore, the two cross coupled inverters will save and retain their current logical value. The word line and bitline are connected through access transistors to read and write to this cross coupled inverter.

2.3 Read Operation

When the wordline is at logical high value, both n- transistors are switched ON and are connected to the inverter inputs and outputs to the two bitlines. It means that, the two inverters force the present data logical value stored in the SRAM cell on the bit line and the inverted data logical value on the inverted-bit line. This data value is then augmented thus generating the output logical value of the 6T memory cell in a read operation. [1]

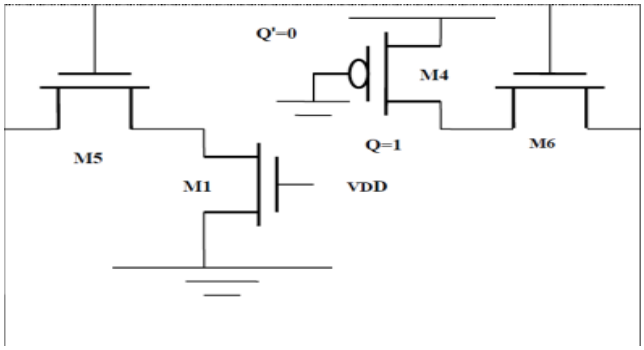

Fig. 2: Read Operation

2.4 Write Operation

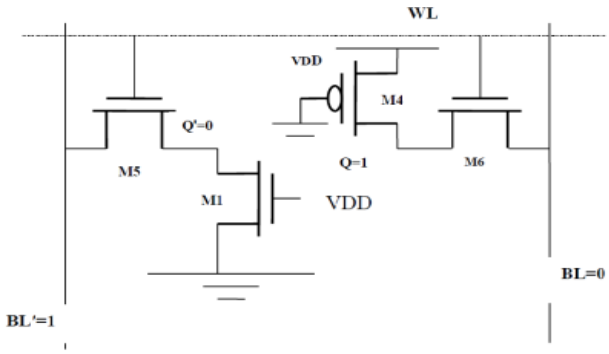

Fig. 3: Write Operation

To inscribe fresh data into the storage cell, the word line is given logical high value, and the bit line drivers are also activated. Based on the present logical value stored in the SRAM cell there may be a short-circuit condition, and the logical value in the storage cell gets overwritten.

3. DESIGN OF 6T SRAM CELL

For calculating W/L ratios of mos transistors in a CMOS SRAM cell design criteria must be taken into consideration:

A) Data read operation should not destroy the store information in the SRAM cell .
B) Cell should allow modification of the stored information during the data write phase.

Data preservation of the memory cell during the read access and standby mode , is an important well-designed constriction in smaller geometry technologies . The memory cell becomes unstable with smaller supply voltage and thus increasing leakage currents and increasing temperature variability, all resulting from technology scaling. The cell stability is defined by the Signal Noise Margin as the highest value of DC noise voltage that can be tolerated by the SRAM cell without altering the stored data bit.

Write margin is defined as the measure of the capability to over write the data into the storage cell. Write margin voltage is the maximum noise voltage value present at bit lines during a correct write operation. When noise voltages exceeds the write margin voltage, then write failure occurs. In this section, we introduce static approach for measuring write margin. [3]

4.1. Simulation Results

The conventional SRAM cell has been tested using SPICE simulations in 0.18 µm standard CMOS TSMC process technology.

Fig. 4 : Read Results

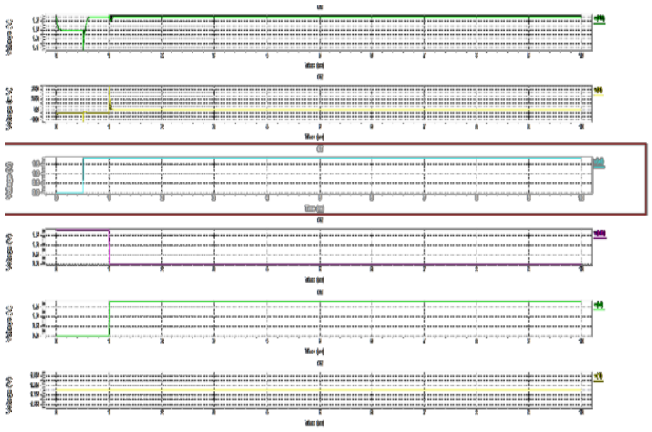

Fig. 5: Write Results

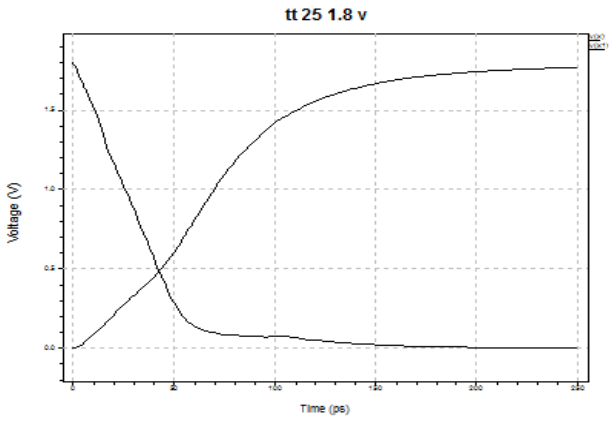

Fig. 6: Butterfly curve for TT, 25 °C, 1.8V

4.2. Characterization Graphs

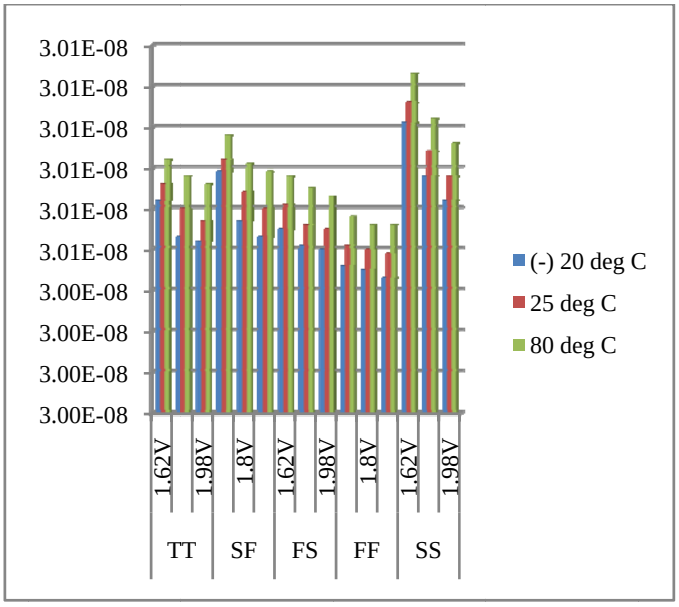

Fig. 7: Read Delay in sec

Following are the characterization graphs for various SRAM parameters across process variations (viz. Typical nMOS – Typical pMOS TT, Slow nMOS - Fast pMOS SF, Fast nMOS - Slow pMOS FS, Fast nMOS –Fast pMOS FF and Slow nMOS -Slow pMOS SS) ; temperature variations (viz. -20 °C, 25 °C and 80°C) and power supply variations of ± 10%.

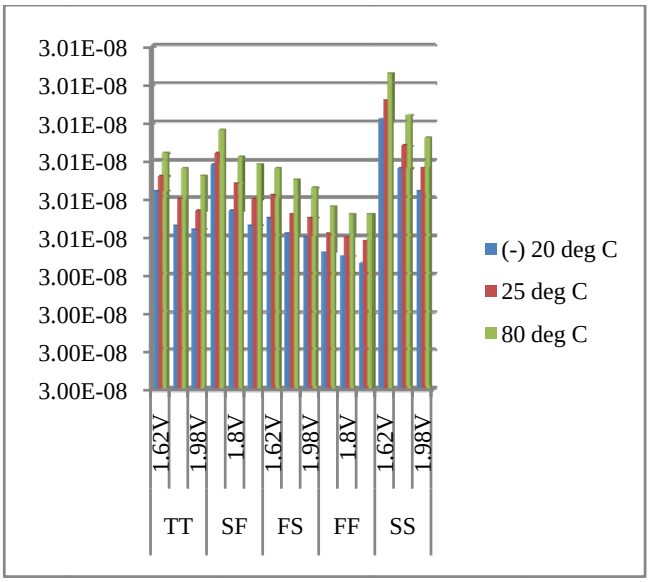

Fig. 8: Write Delay in sec

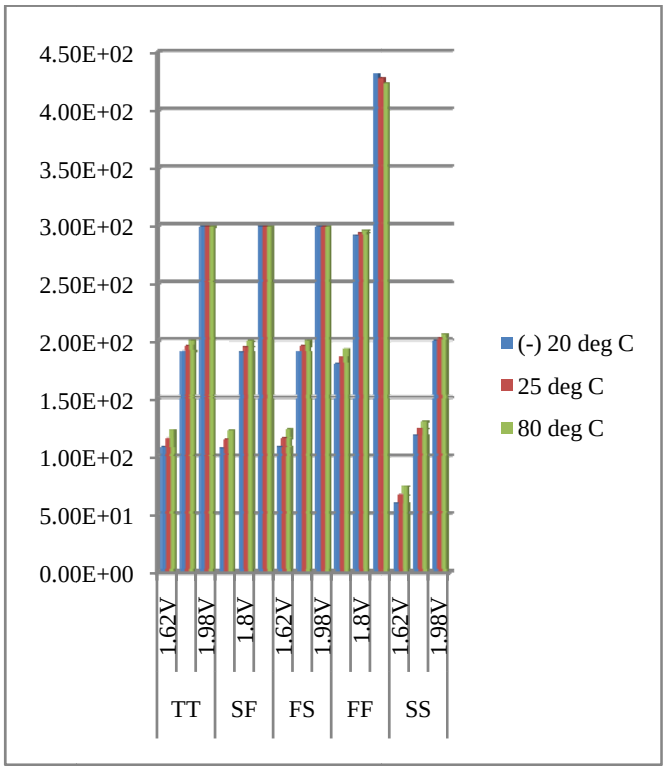

Fig. 9: Leakage Power in µWatts

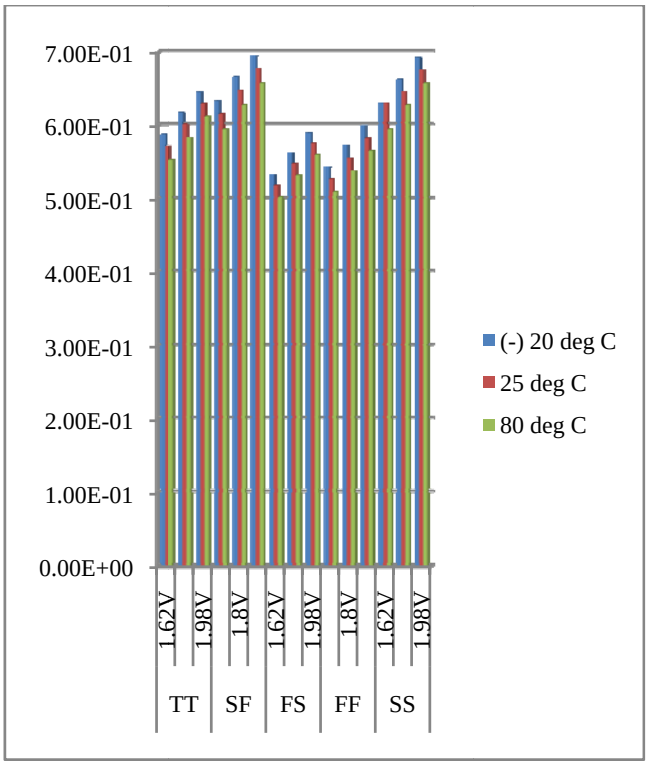

Fig. 10: SNM Read in Volts

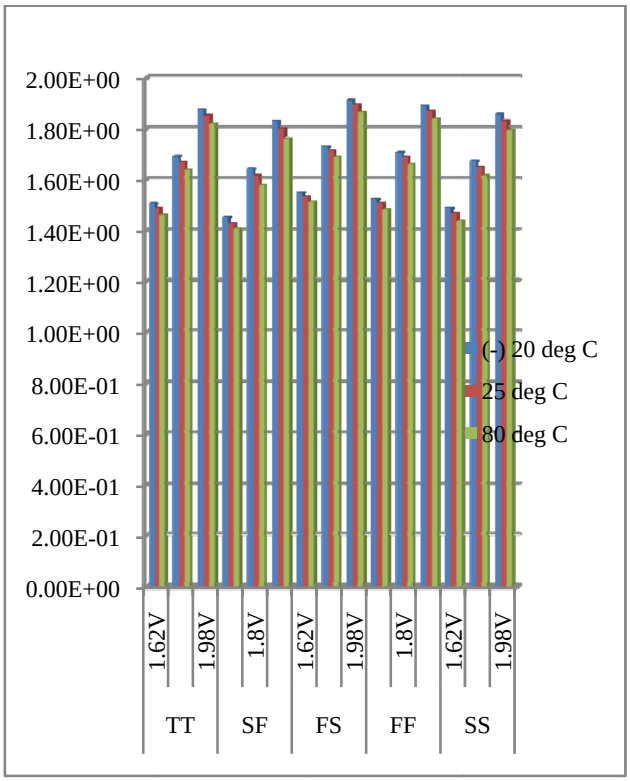

Fig. 11 : SNM Write in Volts

4.3. Results Table

Table 1: Characterization Table

Parameter	Best Case Scenario		Worst Case Scenario	
	O/P Value	Process, Voltage ,Temp	O/P Value	Process, Voltage, Temp
READ Delay (sec)	3E-8	FF,1.98V,-20ºC	3.01E-8	SS, 1.62V,80º C
WRITE Delay (sec)	3E-8	FF,1.98V,-20ºC	3.01E-8	SS, 1.62V,80º C
POWER DISSIPATI —ON	-59.32u	SS,1.62V,-20ºC	-430.87u	FF,.98V,-20ºC
SNM READ (V)	0.658V	SF ,1.98V,80ºC	0.502V	FS,1.62V, 80ºC
SNM WRITE (V)	1.91V	FS,1.98V,-20ºC	1.41V	SF,1.62V, 80ºC

4. CONCLUSION

The presented work performs the analysis and characterization of conventional 6T SRAM cell for the Read and Write operation for high performance, on chip caches memories in 0.18 µm CMOS TSMC process.

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